CLAIMS

What is claimed is:

1. A thermal management system for an integrated circuit die, comprising:
a temperature detection element formed directly on said integrated circuit die, said temperature detection element including at least one temperature sensor having an output;
a power modulation element formed directly on said integrated circuit die and configured to reduce power consumption of said integrated circuit die in response to a logical change in state at said output of said at least one temperature sensor;
a control element formed directly on said integrated circuit die, said control element including at least one register providing an enable/disable bit for said thermal management system; and
a visibility element formed directly on said integrated circuit die and configured to indicate a status of said output of said at least one temperature sensor.

2. The system of claim 1, said at least one temperature sensor comprising:
a reference voltage source providing a reference voltage;
a programmable voltage source providing a programmable voltage proportional to a temperature of said integrated circuit die; and
a comparator having one input coupled via a first signal line to said reference voltage source and another input coupled via a second signal line to said programmable voltage source, said comparator configured to provide said logical change in state at said output of said at least one temperature sensor in response to said programmable voltage substantially equaling said reference voltage.

3. The system of claim 2, further comprising a pulse dampener coupled to said first signal line and configured to at least partially remove electrical noise from said reference voltage.

4. The system of claim 2, further comprising an analog filter coupled to said second signal line and said first signal line, said analog filter configured to detect voltage spikes present in said reference voltage and to add substantially identical voltage spikes to said programmable voltage.

5. The system of claim 2, further comprising a digital filter coupled to an output of said comparator, said digital filter including an up-down counter configured to count clock pulses, said up-down counter configured to increment once for each clock pulse detected when said comparator output is at a logical high and to decrement once for each clock pulse detected when said comparator output is at a logical low.

6. The system of claim 1, said control element further including another register selected from a group consisting of a register configured to selectively disengage a specified portion of said thermal management system, a register configured to enable said thermal management system in response to an occurrence of an external event, a register configured to force said thermal management system active while overriding a disable bit provided by said at least one register, and a register configured to allow external software and hardware to enable said thermal management system.

7. The system of claim 1, said visibility element including at least one device selected from a group consisting of a register configured to indicate said status of said temperature sensor output, a register providing a sticky bit, a counter configured to count a number of lost clock cycles resulting from operation of said thermal management system, and circuitry configured to generate an interrupt when said temperature sensor output transitions to a different logical state.

8. The system of claim 1, said power modulation element configured to lower a supply voltage to said integrated circuit die, lower a frequency of a clock signal provided by internal clock circuitry on said integrated circuit die, perform clock gating of said clock signal provided by said internal clock circuitry, perform clock throttling of said clock signal provided by said internal clock circuitry, selectively block clock pulses of said clock signal provided by said internal clock circuitry, disable at least one of a plurality of functional units on said integrated circuit die, limit instructions sent to at least one of said plurality of functional units on said integrated circuit die, or change a behavior of at least one of said plurality of functional units on said integrated circuit die.

9. A microprocessor, comprising:

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on said die and coupled to at least one of said plurality of functional units; and

a thermal management system formed directly on said die, comprising:

a temperature detection element including at least one temperature sensor having an output;

a power modulation element configured to reduce power consumption of at least one of said functional units in response to a logical change in state at said output of said at least one temperature sensor;

a control element including at least one register providing an enable/disable bit for said thermal management system; and

a visibility element configured to indicate a status of said output of said at least one temperature sensor.

10. The microprocessor of claim 9, said at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of said die; and

a comparator having one input coupled via a first signal line to said reference voltage source and another input coupled via a second signal line to said programmable voltage source, said comparator configured to provide said logical change in state at said output of said at least one temperature sensor in response to said programmable voltage substantially equaling said reference voltage.

11. The microprocessor of claim 10, further comprising a pulse dampener coupled to said first signal line and configured to at least partially remove electrical noise from said reference voltage.

12. The microprocessor of claim 10, further comprising an analog filter coupled to said second signal line and said first signal line, said analog filter configured to detect voltage spikes present in said reference voltage and to add substantially identical voltage spikes to said programmable voltage.

13. The microprocessor of claim 10, further comprising a digital filter coupled to an output of said comparator, said digital filter including an up-down counter configured to count clock pulses, said up-down counter configured to increment once for each clock pulse detected when said comparator output is at a logical high and to decrement once for each clock pulse detected when said comparator output is at a logical low.

14. The microprocessor of claim 9, said control element further including another register selected from a group consisting of a register configured to selectively disengage a specified portion of said thermal management system, a register configured to enable said thermal management system in response to an occurrence of an external event, a register configured to force said thermal management system active while overriding a disable bit provided by said at least one register, and a register configured to allow external software and hardware to enable said thermal management system.

15. The microprocessor of claim 9, said visibility element including at least one device selected from a group consisting of a register configured to indicate said status of said temperature sensor output, a register providing a sticky bit, a counter configured to count a number of lost clock cycles resulting from operation of said thermal management system, and circuitry configured to generate an interrupt when said temperature sensor output transitions to a different logical state.

16. The microprocessor of claim 9, said power modulation element configured to lower a supply voltage to said die, lower a frequency of a clock signal provided by said internal clock circuitry, perform clock gating of said clock signal provided by said internal clock circuitry, perform clock throttling of said clock signal provided by said internal clock circuitry, selectively block clock pulses of said clock signal provided by said internal clock circuitry, disable at least one of said plurality of functional units on said die, limit instructions sent to at least one of said plurality of functional units on said die, or change a behavior of at least one of said plurality of functional units on said die.

17. A computer system, comprising:

at least one memory device coupled to a bus;

at least one microprocessor coupled to said bus and said at least one memory device, said at least one microprocessor comprising:

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on said die and coupled to at least one of said plurality of functional units;

a temperature detection element formed directly on said die, said temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on said die and configured to reduce power consumption of at least one of said functional units in response to a logical change in state at said output of said at least one temperature sensor;

a control element formed directly on said die, said control element including at least one register providing an enable/disable bit for said thermal management system; and

a visibility element formed directly on said die and configured to indicate a status of said output of said at least one temperature sensor, said temperature detection, power modulation, control, and visibility elements comprising a thermal management system for said die.

18. The computer system of claim 17, said at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of said die; and

a comparator having one input coupled via a first signal line to said reference voltage source and another input coupled via a second signal line to said programmable voltage source, said comparator configured to provide said logical change in state at said output of said at least one temperature sensor in response to said programmable voltage substantially equaling said reference voltage.

19. The computer system of claim 18, further comprising a pulse dampener coupled to said first signal line and configured to at least partially remove electrical noise from said reference voltage.

20. The computer system of claim 18, further comprising an analog filter coupled to said second signal line and said first signal line, said analog filter configured to detect voltage spikes present in said reference voltage and to add substantially identical voltage spikes to said programmable voltage.

21. The computer system of claim 18, further comprising a digital filter coupled to an output of said comparator, said digital filter including an up-down counter configured to count clock pulses, said up-down counter configured to increment once for each clock pulse detected when said comparator output is at a logical high and to decrement once for each clock pulse detected when said comparator output is at a logical low.

22. The computer system of claim 17, said control element further including another register selected from a group consisting of a register configured to selectively disengage a specified portion of said thermal management system, a register configured to enable said thermal management system in response to an occurrence of an external event, a register configured to force said thermal management system active while overriding a disable bit provided by said at least one register, and a register configured to allow external software and hardware to enable said thermal management system.

23. The computer system of claim 17, said visibility element including at least one device selected from a group consisting of a register configured to indicate said status of said temperature sensor output, a register providing a sticky bit, a counter configured to count a number of lost clock cycles resulting from operation of said thermal management system, and circuitry configured to generate an interrupt when said temperature sensor output transitions to a different logical state.

24. The computer system of claim 17, said power modulation element configured to lower a supply voltage to said die, lower a frequency of a clock signal provided by said internal clock circuitry, perform clock gating of said clock signal provided by said internal clock circuitry, perform clock throttling of said clock signal provided by said internal clock circuitry, selectively block clock pulses of said clock signal provided by said internal clock circuitry, disable at least one of said plurality of functional units on said die, limit instructions sent to at least one of said plurality of functional units on said die, or change a behavior of at least one of said plurality of functional units on said die.

25. A method of performing thermal management on a microprocessor, comprising:

providing an enable bit to a register of a thermal management system to activate said thermal management system;

measuring a temperature on a die of said microprocessor with a sensor of said thermal management system;

providing a logical low at an output of said sensor when said temperature is below a trip point;

providing a logical high at said sensor output when said temperature equals or exceeds said trip point;

engaging a power reduction mechanism to reduce power consumption of said die in response to said logical high at said sensor output; and

providing an indication of a logical status of said output of said sensor to an external device.

26. The method of claim 25, said engaging a power reduction mechanism comprising an act selected from a group consisting of lowering a supply voltage to said die, lowering a frequency of a clock signal provided by internal clock circuitry of said microprocessor, performing clock gating of said clock signal provided by said internal clock circuitry, performing clock throttling of said clock signal provided by said internal clock circuitry, selectively blocking clock pulses of said clock signal provided by said internal clock circuitry, disabling at least one of a plurality of functional units on said microprocessor, limiting instructions sent to at least one of said plurality of functional units on said microprocessor, and changing a behavior of at least one of said plurality of functional units on said microprocessor.

27. The method of claim 25, said providing an enable bit to a register of said thermal management system comprising providing an enable bit to said register from an external operating system.

28. The method of claim 25, further comprising:
engaging said power reduction mechanism for a specified time period;
polling said sensor output after expiration of said specified time period;
engaging said power reduction mechanism for at least another said specified time period when said sensor output exhibits said logical high; and
halting said power reduction mechanism when said sensor output exhibits said logical low;

29. The method of claim 25, further comprising:
engaging said power reduction mechanism for a specified time period;
continuously polling said sensor output after expiration of said specified time period; and
halting said power reduction mechanism when said sensor output exhibits said logical low.

30. The method of claim 25, further comprising:
providing said logical low at said sensor output when said temperature is below an untrip point, said untrip point less than said trip point; and
halting said power reduction mechanism in response to said logical low.

31. The method of claim 25, further comprising:
coupling an up-down counter to said sensor output;
incrementing said up-down counter once for every clock pulse of said clock signal provided by said internal clock circuitry when said sensor output exhibits said logical high; and
decrementing said up-down counter once for every clock pulse of said clock signal provided by said internal clock circuitry when said sensor output exhibits said logical low.

32. The method of claim 25, further comprising:
defining a plurality of trip temperatures, a highest of said plurality of trip temperatures corresponding to said trip point;
assigning a plurality of duty cycle values to said plurality of trip temperatures, one duty cycle value of said plurality of duty cycle values corresponding to at least one of said plurality of trip temperatures; and
providing a clock signal from said internal clock circuitry exhibiting said one duty cycle value in response to said temperature substantially equaling said at least one corresponding trip temperature.

33. The method of claim 25, further comprising counting a number of clock cycles eliminated from an output of said internal clock circuitry resulting from said engaging a power reduction mechanism.

34. An apparatus, comprising:
a temperature detection element, said temperature detection element including at least one temperature sensor having an output;
a power modulation element, said power modulation element to reduce power consumption of an integrated circuit die in response to a logical change in state at said output of said at least one temperature sensor;
a visibility element, said visibility element to indicate a status of said output of said at least one temperature sensor, said visibility element comprising:
a register to indicate said status of said temperature sensor output;
a register providing a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of said apparatus; and
circuitry to generate an interrupt when said temperature sensor output transitions to a different logical state.

35. The apparatus of claim 34, further including a control element, said control element comprising:

a register providing an enable/disable bit for said apparatus;

a register configured to selectively disengage a specified portion of said apparatus;

a register configured to enable said apparatus in response to an occurrence of an external event;

a register configured to force said apparatus active while overriding a disable bit provided at said enable/disable bit; and

a register configured to allow external software and hardware to enable said apparatus.

36. The system of claim 34, said power modulation element configured to lower a supply voltage to said integrated circuit die, lower a frequency of a clock signal provided by internal clock circuitry on said integrated circuit die, perform clock gating of said clock signal provided by said internal clock circuitry, perform clock throttling of said clock signal provided by said internal clock circuitry, selectively block clock pulses of said clock signal provided by said internal clock circuitry, disable at least one of a plurality of functional units on said integrated circuit die, limit instructions sent to at least one of said plurality of functional units on said integrated circuit die, or change a behavior of at least one of said plurality of functional units on said integrated circuit die.